Participation in ALICE upgrade

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For ALICE-INDIA Collaboration

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Participation in ALICE upgrade

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ALICE Upgrade Overview

Planned for 2018 (LHC 2nd Long Shutdown)

("Upgrade of the ALICE Experiment", LoI, CERN-LHCC-2012-12)

Physics goals

- Heavy Flavor
- Quarkonia
- Low-mass dielectrons
- Jets
- Anti- and Hypernuclei

Target

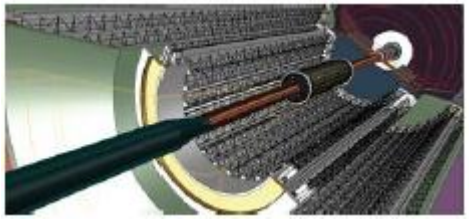
- Pb-Pb recorded luminosity $\geq 10\ nb^{-1}$ => 8×10^{10} events
- pp (@5.5 Tev) recorded luminosity $\geq 6\ pb^{-1}$ => 1.4×10^{11} events

ALICE Before LS2	ALICE After LS2
$L = 10^{27}\ cm^{-2}\ s^{-1}$	$L = 6 \times 10^{27}\ cm^{-2}\ s^{-1}$
$1\ nb^{-1}$ Pb Pb Collisions	> $10\ nb^{-1}$ of Pb Pb collisions
Collision rate of 8 kHz (PbPb)	Collision rate of 50 kHz (PbPb)
Max Readout rate of present ALICE detector is 500 Hz (PbPb)	Overall goal to readout 50 kHz (PbPb) and 200 kHz (pp and pPb)

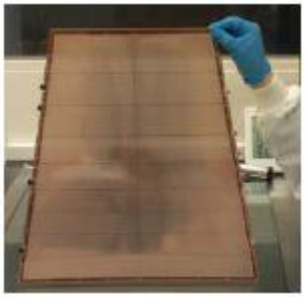
ALICE Upgrade Overview

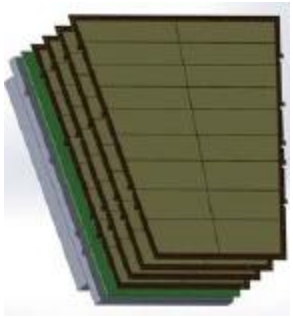
The upgrade plan entails building

- New, high-resolution, low-material ITS
- **Upgrade of TPC with replacement of MWPCs with GEMs and new pipelined readout electronics**
- **Upgrade of readout electronics of: TRD, TOF, PHOS**
- **Upgrade of readout electronics of the Muon Spectrometer**
- Upgrade of the forward trigger detectors and ZDC
- Muon Forward Tracker (MFT)
- **Upgrade of the online systems**
- **Upgrade of the offline reconstruction and analysis framework and code**



CRU





TPC-GEM

ALICE Upgrade Overview

Requirements:

Sample full 50kHz Pb-Pb interaction rate
(current limit at ~500Hz, factor 100 increase)
Typical event size of PbPb collisions@5.5TeV: 22 Mbyte
=> ~1.1 TByte/s detector readout
=> ~500 PByte/HI period (1 month)

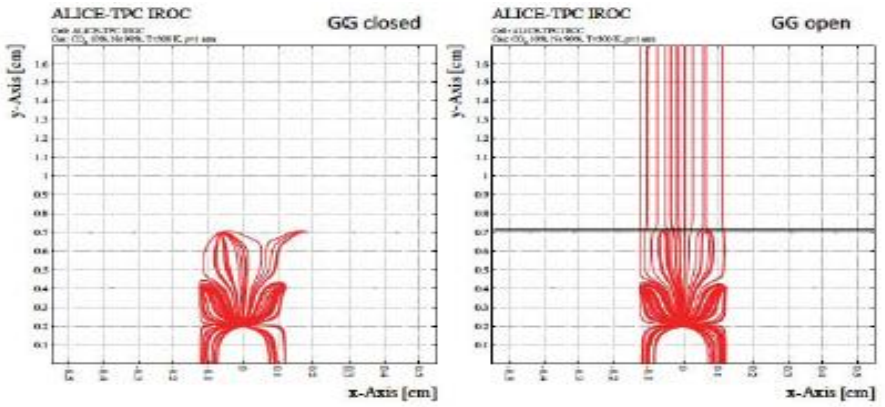
However:

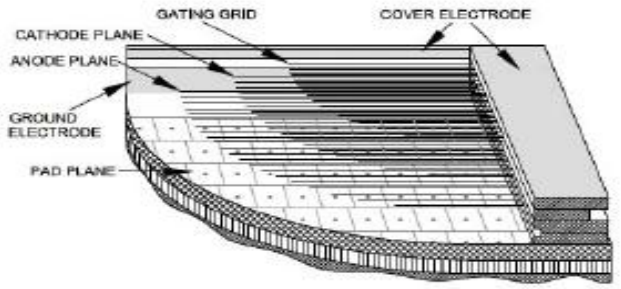
storage bandwidth limited to ~20 GByte/s
How to reduce the data rate? Trigger?!?

Triggering on D0, Ds and Λc (pT>2 Gev/c)
=> **~ 20-25kHz@50kHz rate..**

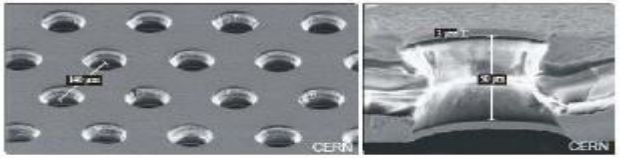
Particle	Eff	S/ev	S/B	B'/ev	trigger rate (Hz)	S/nb^{-1}
D^0	0.02	$1.6 \cdot 10^{-3}$	0.03	0.21	$11 \cdot 10^3$	$1.3 \cdot 10^7$
D_s^+	0.01	$4.6 \cdot 10^{-4}$	*0.01*	0.18	$9 \cdot 10^3$	$3.7 \cdot 10^6$
Λ_c	0.01	$1.4 \cdot 10^{-4}$	$5 \cdot 10^{-5}$	11	$5 \cdot 10^4$	$1.1 \cdot 10^6$
Λ_c ($p_t > 2$ GeV/c)	0.01	$0.8 \cdot 10^{-4}$	0.001	0.33	$1.6 \cdot 10^4$	$0.6 \cdot 10^6$
$B \to D^0(\to K^-\pi^+)$	0.02	$0.8 \cdot 10^{-4}$	0.03	$11 \cdot 10^{-3}$	$5 \cdot 10^2$	$0.6 \cdot 10^6$
$B \to J/\psi(\to e^+e^-)$	0.1	$1.3 \cdot 10^{-5}$	*0.01*	$5 \cdot 10^{-3}$	$3 \cdot 10^2$	$1 \cdot 10^5$
$B^+ \to J/\psi K^+$	*0.01*	$0.5 \cdot 10^{-7}$	*0.01*	$2 \cdot 10^{-5}$	1	$4 \cdot 10^2$
$B^+ \to \overline{D}^0\pi^+$	*0.01*	$1.9 \cdot 10^{-7}$	*0.01*	$8 \cdot 10^{-5}$	4	$1.5 \cdot 10^3$
$B_s^0 \to J/\psi\phi$	*0.01*	$1.1 \cdot 10^{-8}$	*0.01*	$4.4 \cdot 10^{-6}$	$2 \cdot 10^{-1}$	$9 \cdot 10^1$
$\Lambda_b(\to \Lambda_c + e^-)$	*0.01*	$0.7 \cdot 10^{-6}$	*0.01*	$2.8 \cdot 10^{-4}$	14	$5 \cdot 10^3$
$\Lambda_b(\to \Lambda_c + h^-)$	*0.01*	$0.7 \cdot 10^{-5}$	*0.01*	$2.8 \cdot 10^{-3}$	$1.4 \cdot 10^2$	$5 \cdot 10^4$

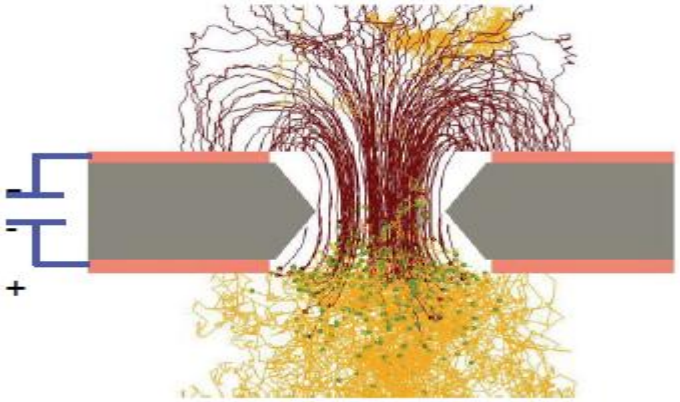
ALICE TPC upgrade





Ions from the amplification region require finite drift time to reach the gating grid
With current ALICE TPC gas: ~100 µs drift + 180 ~µs gating grid closing time
Rate limited to ~3.5 kHz



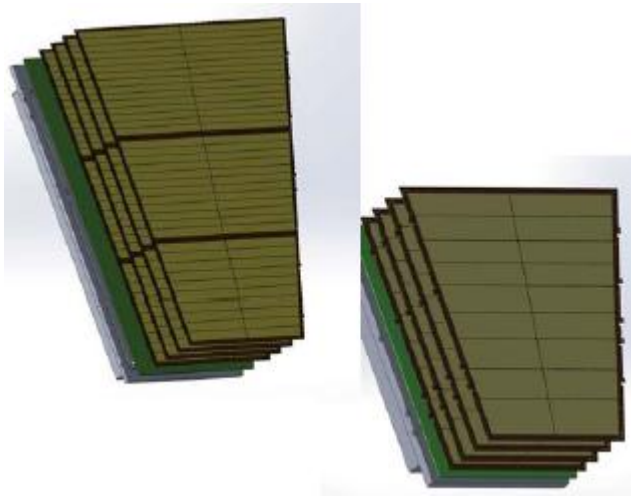


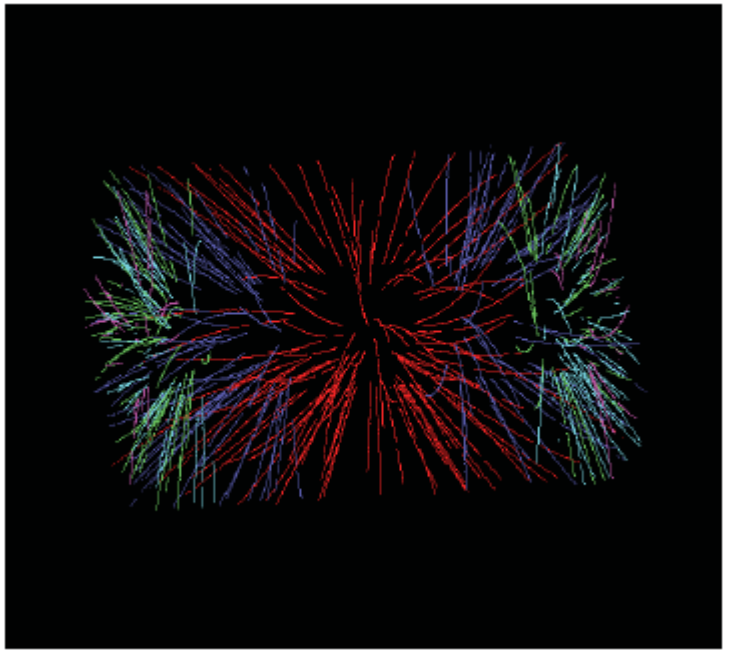
GEM: Gas Electron Multiplier

- copper – kapton – copper sandwich (~50µm) with holes etched into it
- large field strength inside holes, sufficient for avalanche creation (gas amplification)
- fast negative signal (**new electronics**)
- **asymmetric field configuration features intrinsic ion blocking**

ALICE TPC upgrade

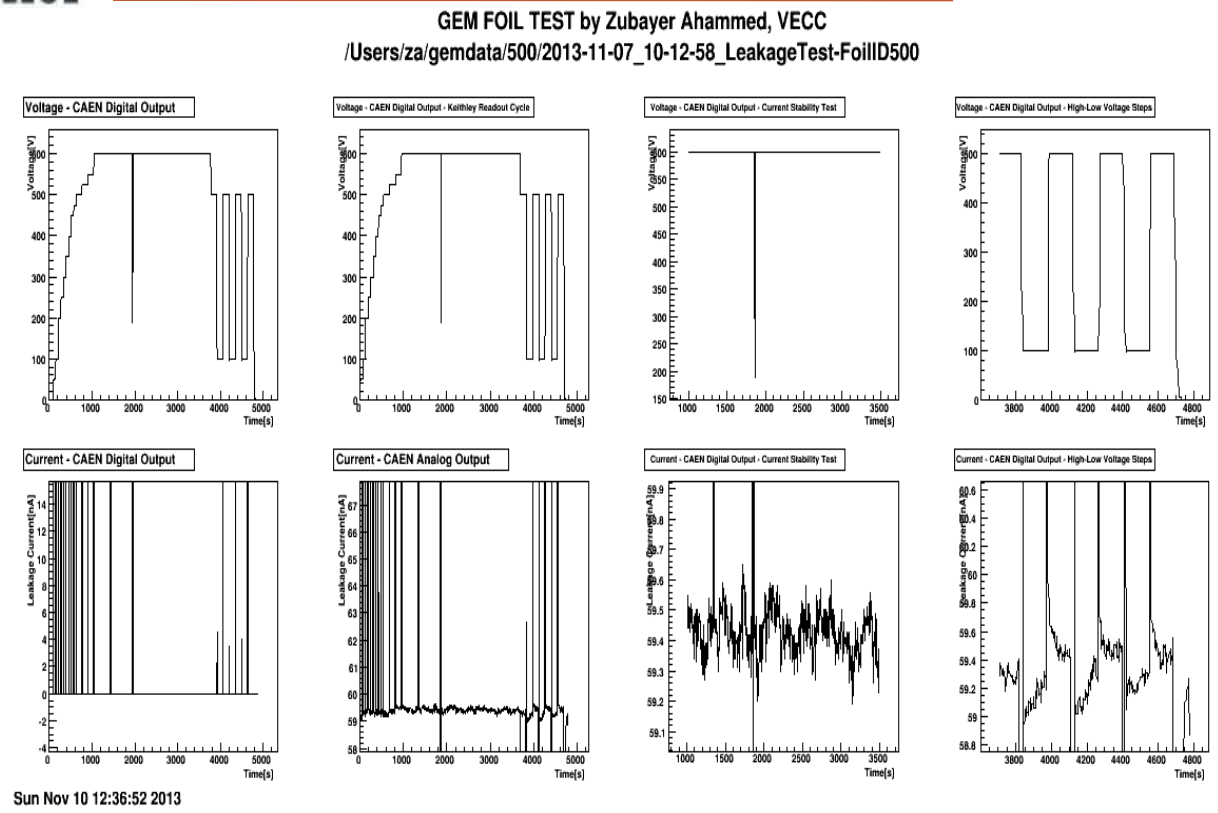
New read-out chambers based on 4 GEM layer setup





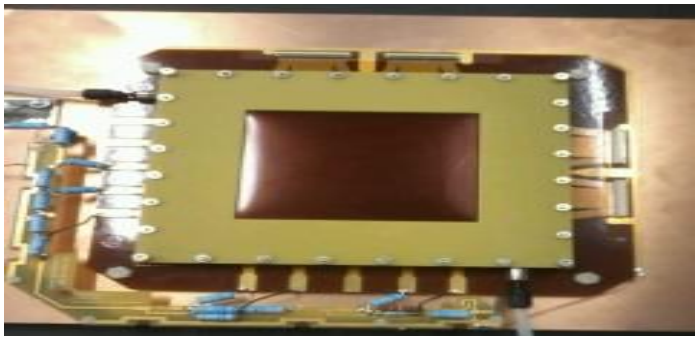
Operated in continuous mode: **self triggered electronic**
At 50kHz: on average 5 events in TPC drift time of ~100 µs
-> Factor 5 in data volume for online systems to read-out and process

Our participation:: Characterization of GEM Foils



Material : three sets of:
Size: 10 cm X 10 cm
Double Mask
Pitch: 140 µm, 280 µm
Thickness: 0.5 mm
Hole diameter: 70 µm
Di-electric: Polymide (KAPTON)

Nine Foils are tested
Voltage applied 600V
Stability with 0.1 nA.
No. of Discharges are ~1

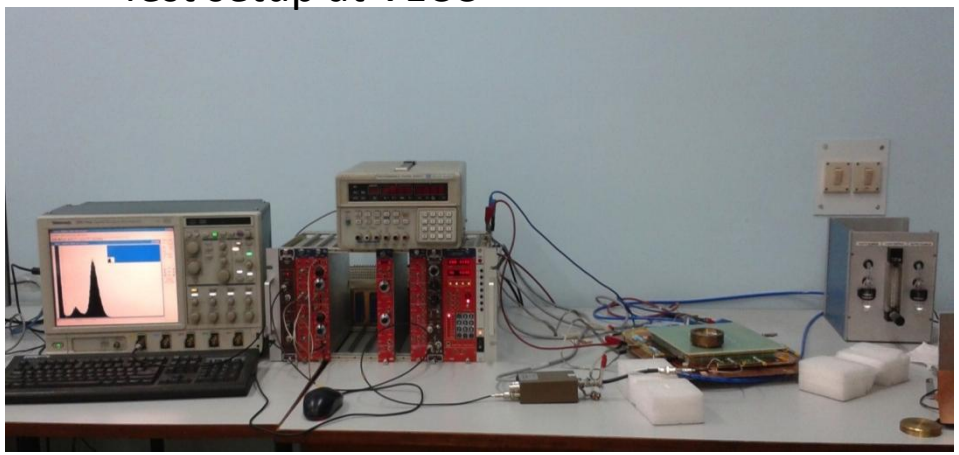


First Prototype made at CERN and tested at VECC

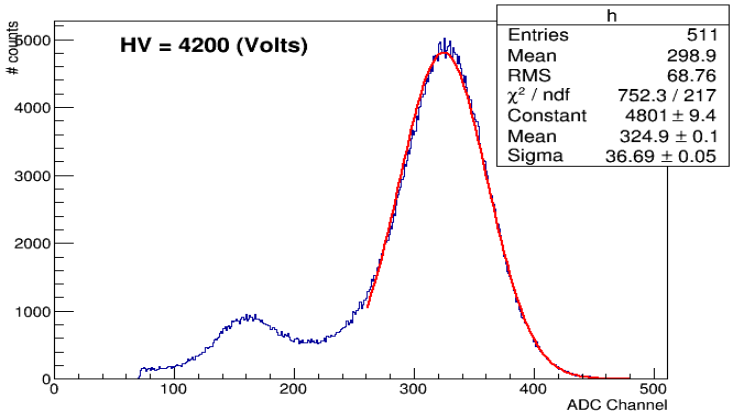
- Triple GEM (10cm X10cm)
  - Gas Gap: 3-2-2-2 mm
  - Δv1= 397 Volts
  - ΔV2= 364 volts
  - ΔV3= 323 Volts

Our participation:: Response of the Detector

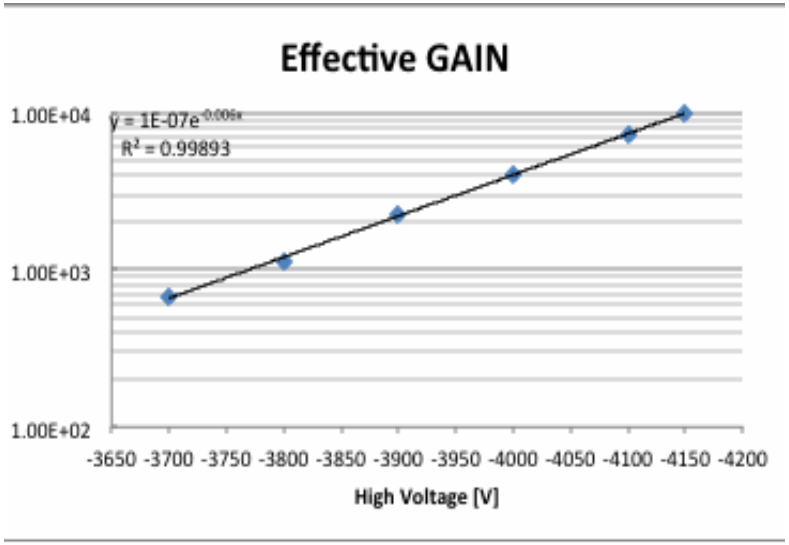
Test setup at VECC



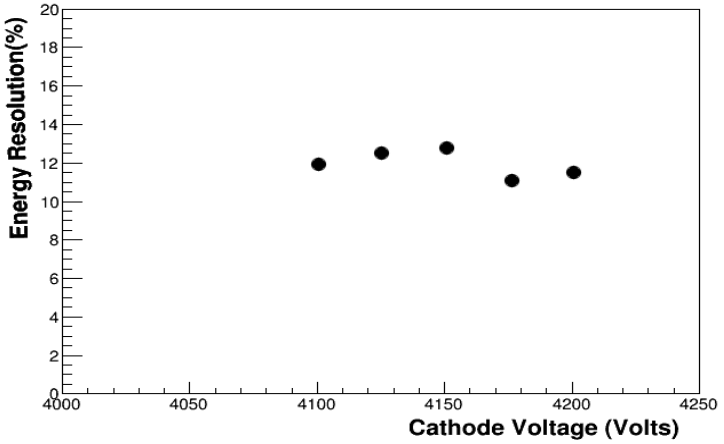
Signal with Fe-55



Gain ~ 10^4



Energy Resolution ~ 12%



Detector Readout

Combination of continuous and triggered readout

Continuous readout for TPC (and ITS)

- At 50 kHz, ~5 events in TPC during drift time of ~100 μs Continuous readout minimizes needed bandwidth
- Implies change from event granularity in the online systems to time-windows with multiple events
- Implies event building only after partial reconstruction. Fast Trigger Processor (FTP) complementing CTP
- Provides clock/L0/L1 to triggered detectors and TPC/ITS for data tagging and test purposes

DDL/RORC Development

Data Link

DDL1 (Run 1): 2Gbit/s

DDL2 (Run 2): 6 Gbit/s

DDL3 (LS2): 10 Gbit/s

Receiver Card (FPGA)

- RORC1 (now)

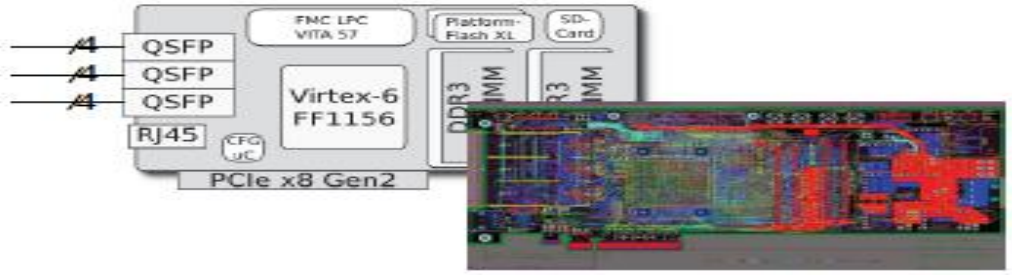
2 DDL1, PCI-X&PCIe Gen1x4

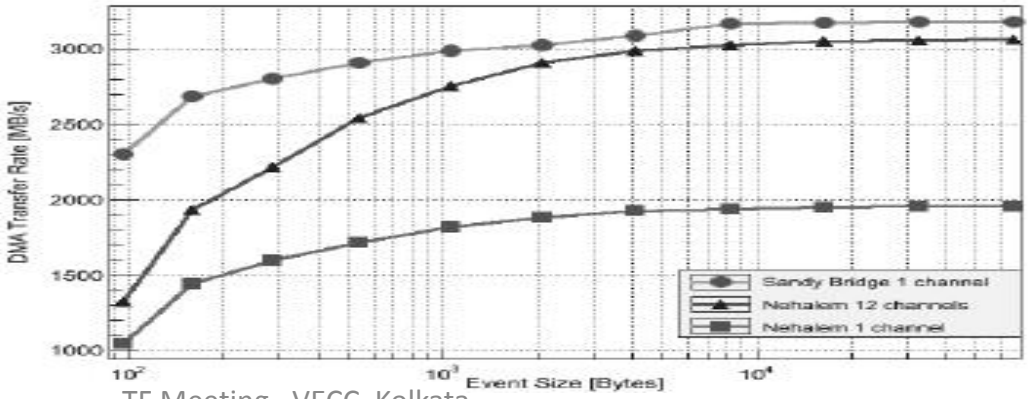
- RORC2 (being produced)

12 DDL2, PCIe Gen2x8

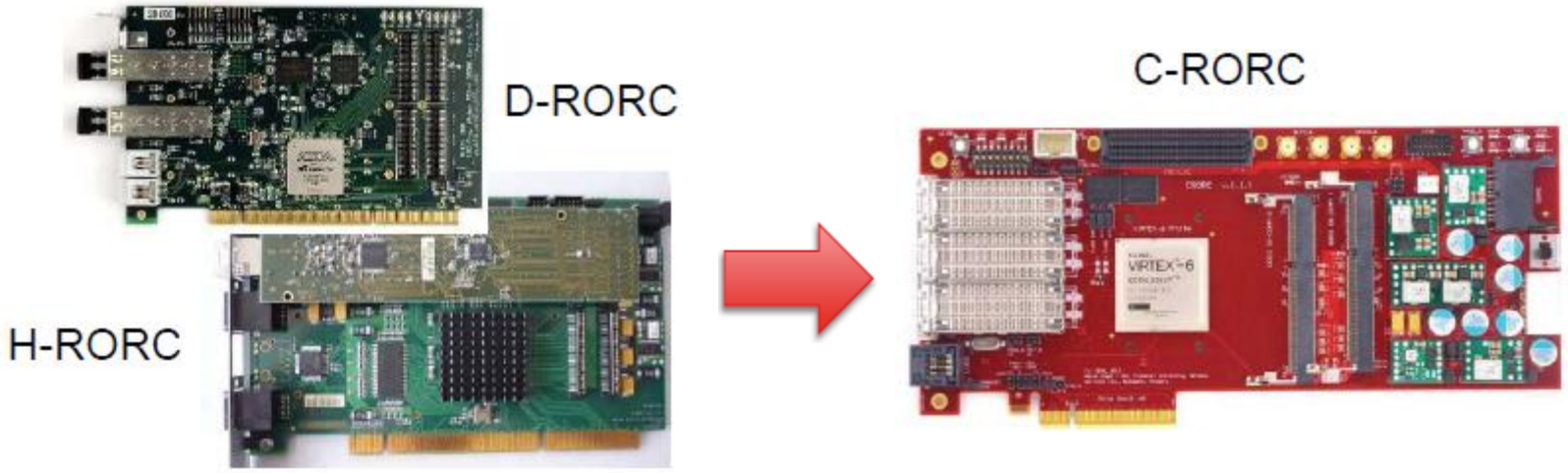
- **RORC3 (LS2)**

10-12 DDL3, PCIe Gen3





Read-Out Receiver Card



Common Read-Out Receiver Card

- mainly developed by IRI Frankfurt&Cerntech for HLT Run 2
- in production now, delivery this year

Increased link speed: **2 Gb/s (DDL1) -> 6 Gb/s (DDL2)**

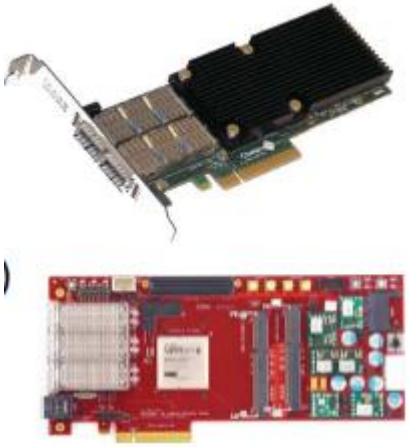
Increased number of ports: **2 -> 12**

Detector Readout

Run 3 Detector Readout

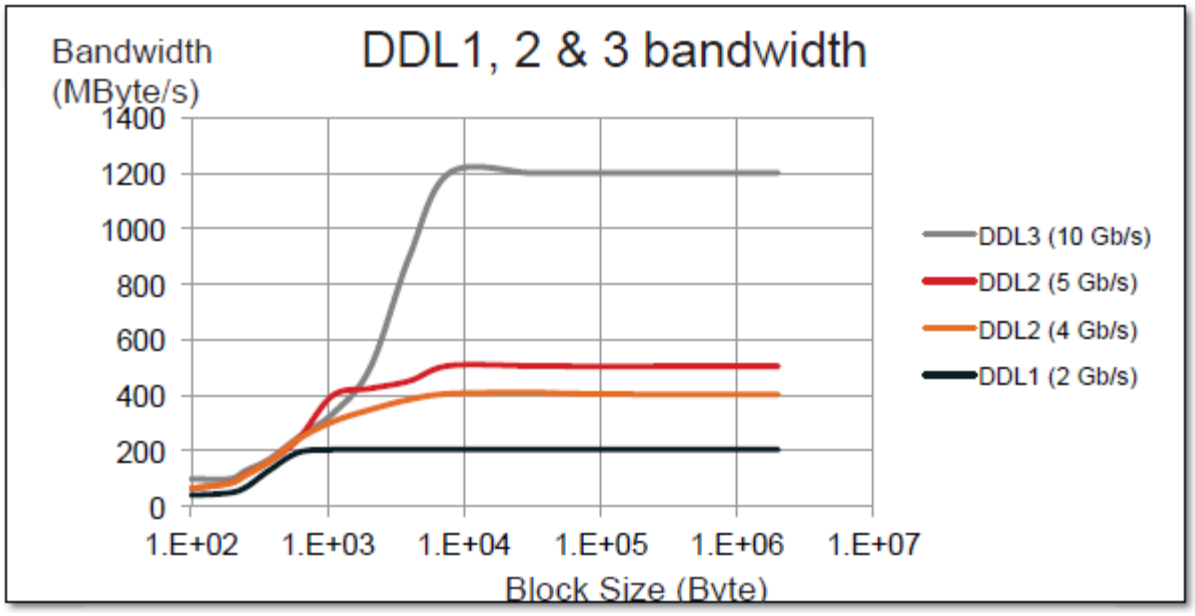
Different link protocols under investigation:

– DDL3 (custom, 10Gb/s)
– Ethernet (10 - 40 Gb/s)
– PCIe over cable (Gen2, Gen3; 16 - 128 Gb/s)
– GBT (3 – 4 Gb/s)



- Large variation in link bandwidths
- Number of links and FLPs depend upon decision about read-out implementation
- Data compression by co-processing (FPGA or other)
- Run 1 and 2: combined in a custom card with DDL receiver
- Run 3: could we split the dataflow and the data processing ?
- Benchmark of memory bandwidth
- S/W compression on FLP?

DDL Performance Evolution



- DDL2 at 4 and 5 Gb/s (according to needs) ready for Run 2
- Prototype for one of the DDL3 option considered for Run 3
- implemented (Eth. + UDP/IP)
- Expected performance evolution verified

CONSTRAINTS FOR A COMMON READOUT UNIT

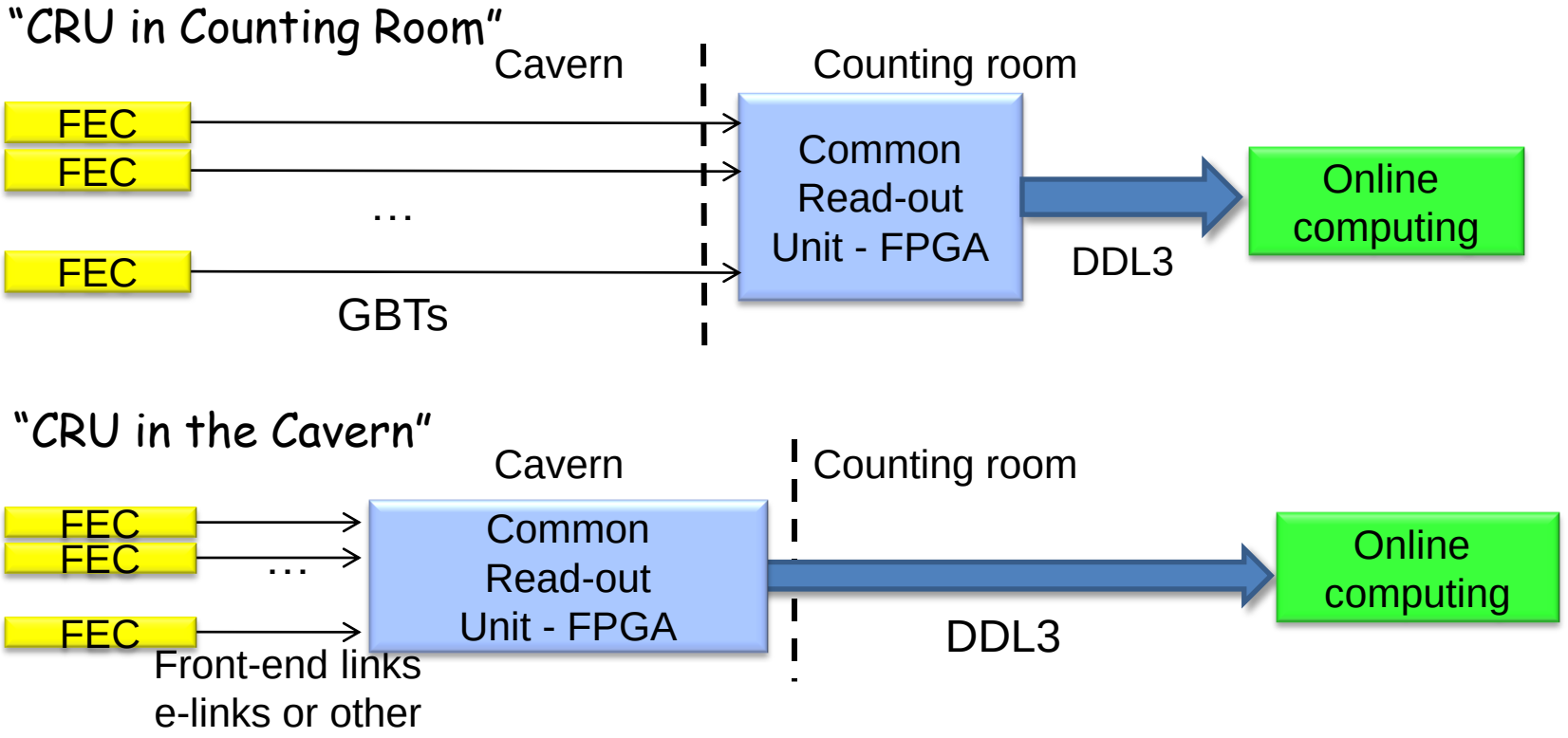
- To preserve smart features of the present DAQ system, like:
  1. Common interfaces between the various detectors and the common Online computing farm.
  2. Optimizing the system level costs by aggregating the digital data from very high number of sources to high bandwidth optical data links.
- In the present system, data transmission through two generations of Detector Data Links (DDL1 and DDL2)
- DDL3 links, higher data throughput requirements of operation in Run3

FEATURES OF THE CRU

- Reduce the number of different link technologies presently used for the data read-out, detector control, trigger and clock distribution, etc.
- Read-out the very large number high bandwidth, serial detector side links, and multiplex to common, even higher bandwidth, server-side links ('uplinks', or 'DDL3').
- Minimize the number of physical links between the different nodes of the system

Our Participation :: IMPLEMENTATION PLANNING

- The application specific functionalities, require Common Read-out Units be implemented as electronics boards with custom designed, programmable functionality based on up-to-date FPGA technology
- Two basic alternatives, depending on the physical location of the CRUs.

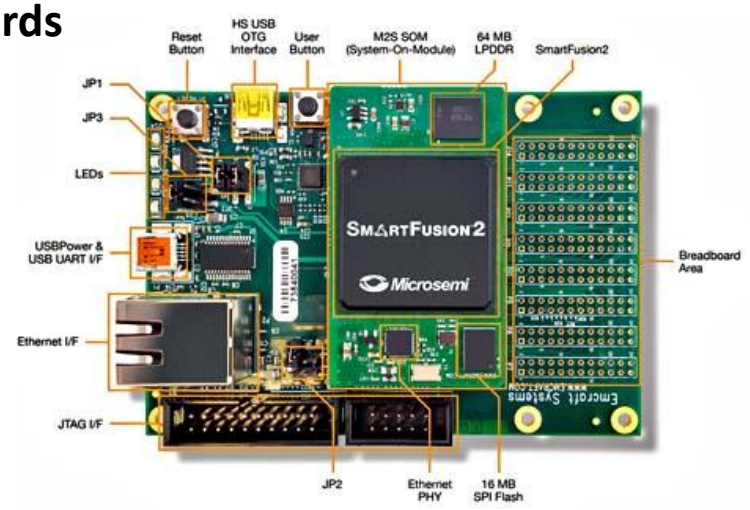


Our Participation :: IMPLEMENTATION PLANNING

Study on Possible FPGAs

CRU in Counting Room	CRU in Cavern
Xilinx Virtex 7 or Altera Stratix V GX Not radiation Tolerant SRAM based FPGAs	Microsemi Smart Fusion 2 Radiation Tolerant Flash memory based FPGA

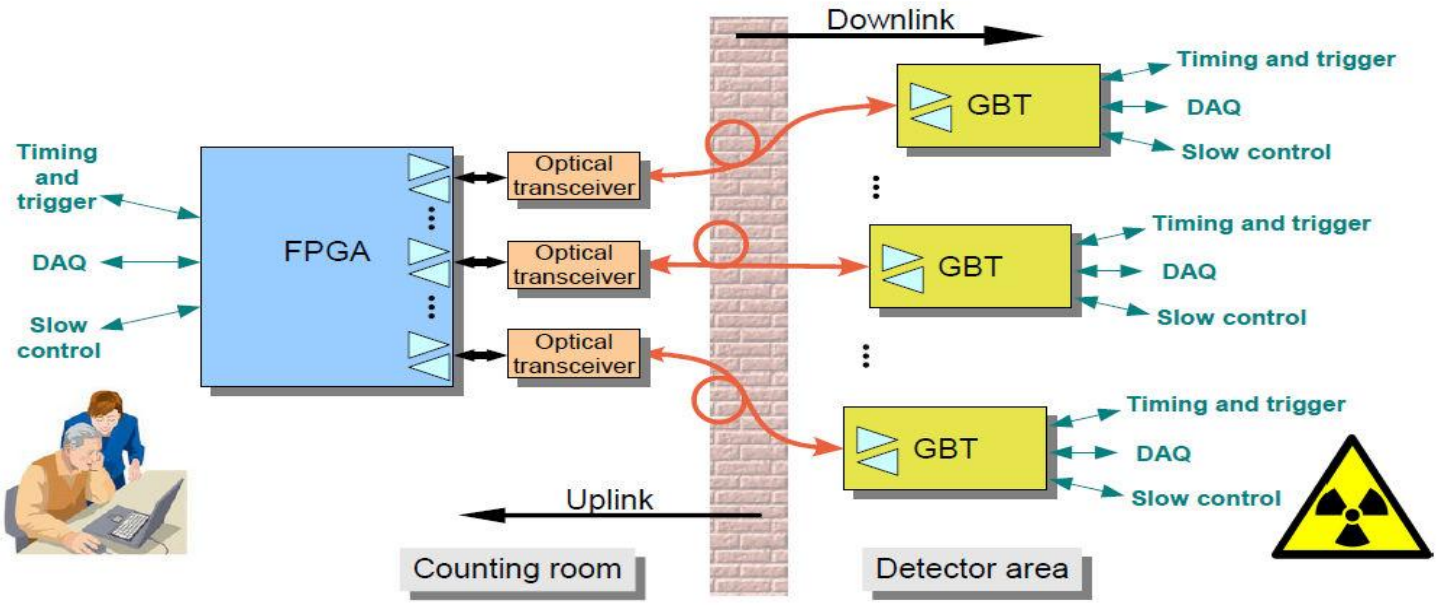
FPGA development boards



Our Participation :: IMPLEMENTATION PLANNING

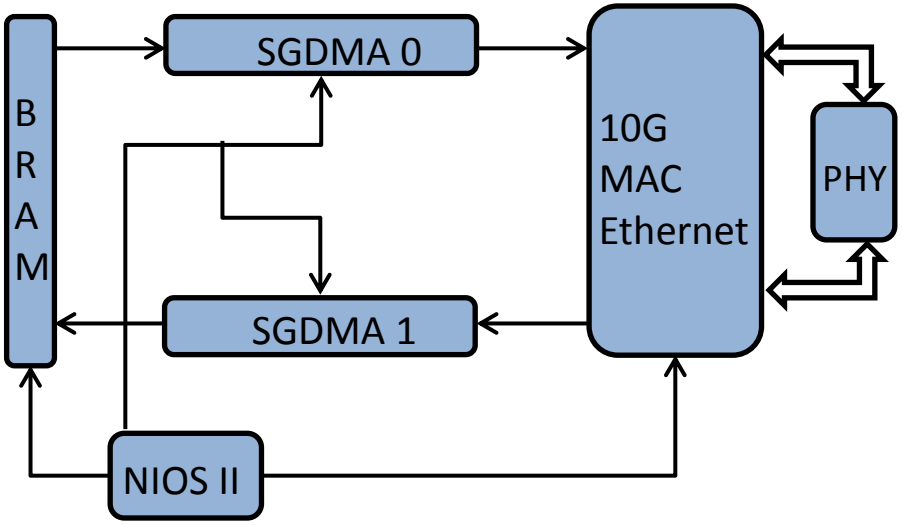
CRU in the Counting room - with GBT Links

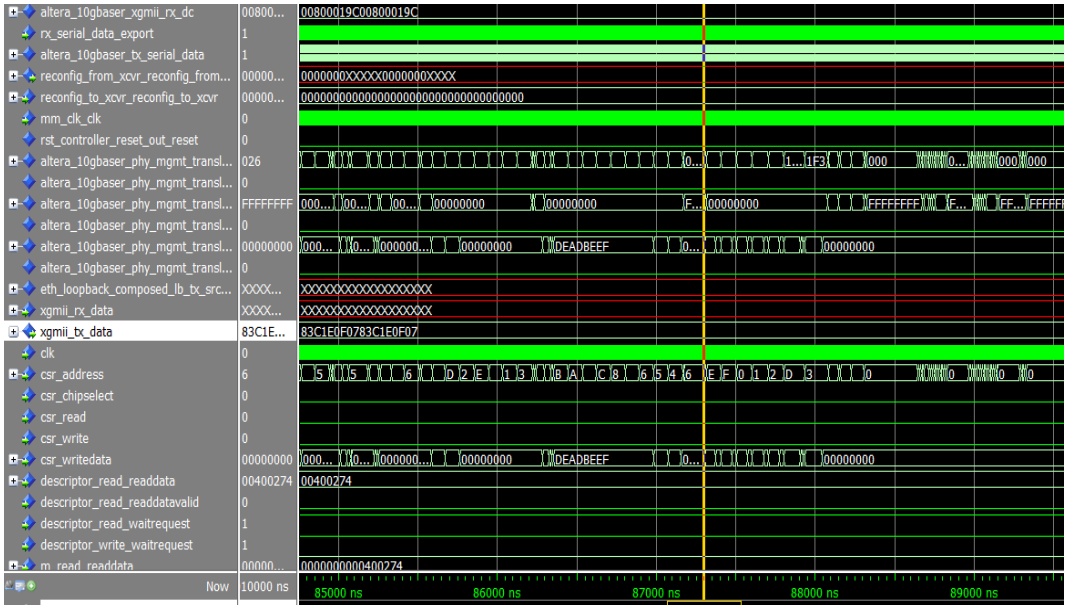
- Located in the control room, CRU doesn't have to be radiation tolerant.
- Detector systems are connected to the CRU via radiation hard optical links developed at CERN, called GBT Links.
- If automatic SEU error correction is activated in GBT, the link bandwidth is 3.2 Gb/s or 4.8 Gb/s



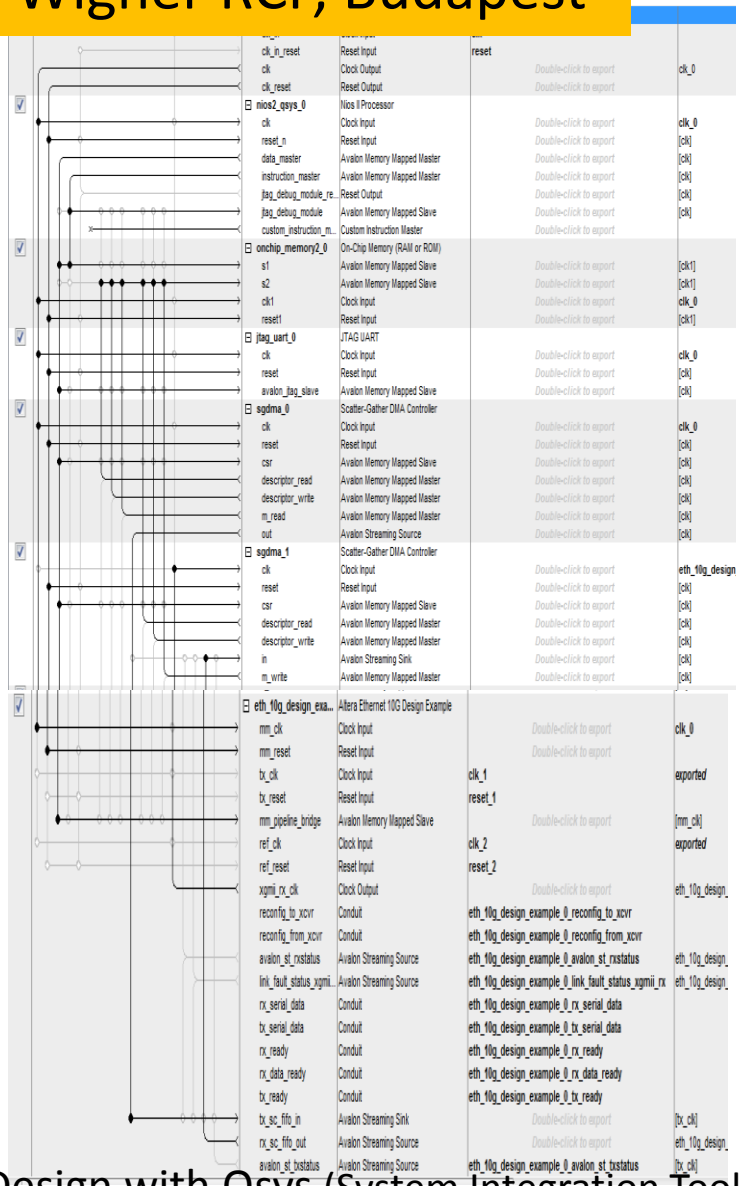
Our Participation :: 10Gbs Ethernet Communication

Development with Wigner RCP, Budapest





Simulation Waveform in Modelsim



Design with Qsys (System Integration Tool)

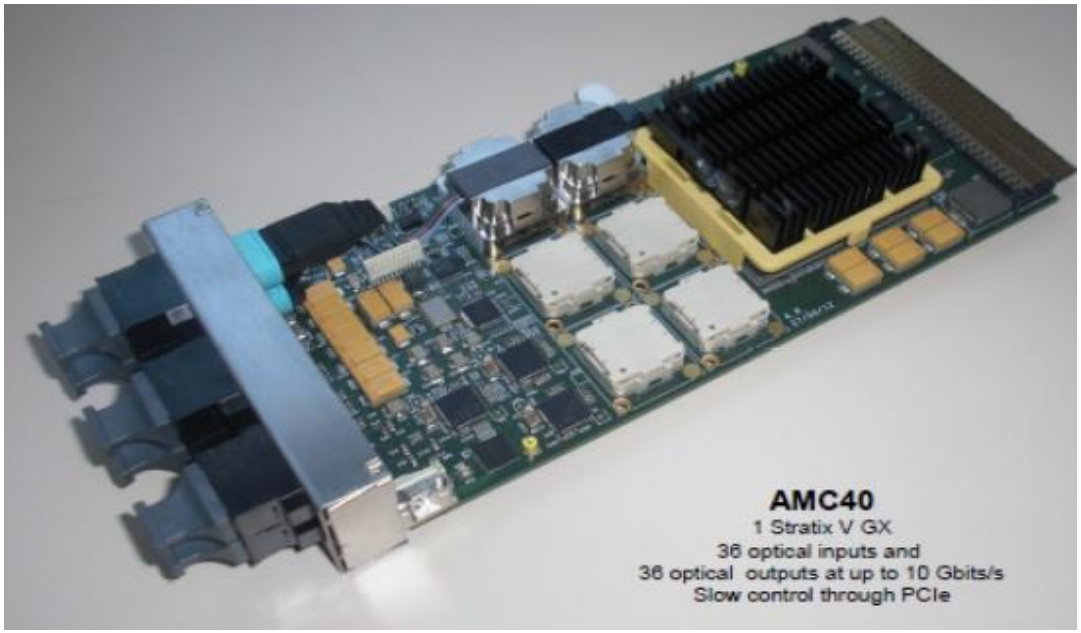
Our Participation :: CRU

AMC40 AS A CANDIDATE FOR THE CRU

- ALICE CRU system is based on the hardware implementation basis of the AMC40/TELL40 system developed in the framework of the LHCb readout.

- Each AMC40 board has 36 optical inputs and 36 optical outputs with a bandwidth upto 10 Gb/s.

- Option to pack the CRU, instead into ATCA form factor with optical link connection, to the Online computing nodes with PCIe slots on the nodes. (DDL3 link will not be needed)



AMC40 mezzanine card

Our Participation :: CRU

SOME Steps :

- Design exploration for the prototype is underway
- Received one AMC40 card from LHCb for further analysis and examination
- Design for 10 Gigabit Ethernet communication to be tested
- GBT receiver to be implemented
- A firmware design framework for detector specific firmware development has to specified

Decided Deadlines:

2013/14: Design specification & market evaluation

2014/15: Common CRU firmware and Prototyping

2015: Pre-series

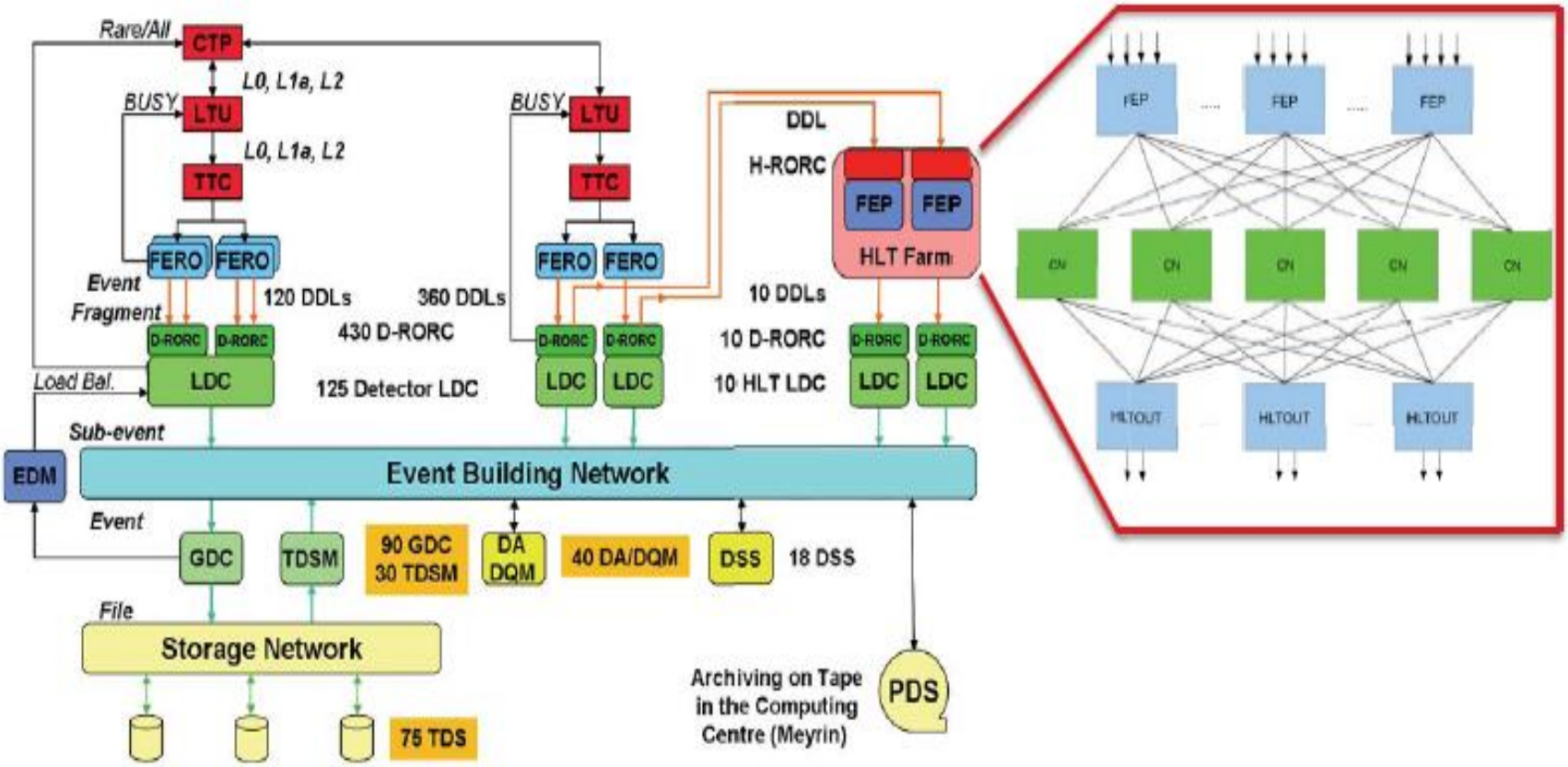
2016: Production

2018: HW & Firmware Support

2018: Installation & Commissioning

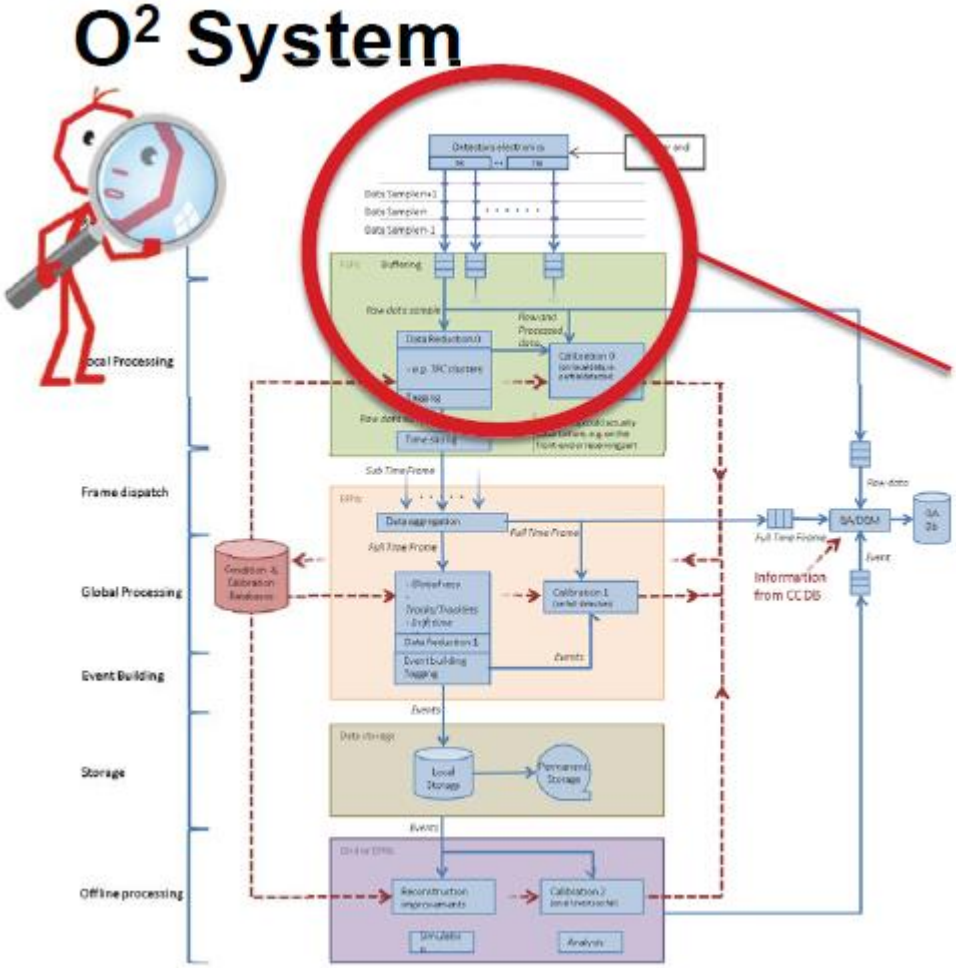
Overview of Online-Offline (O^2)

Current Online Systems

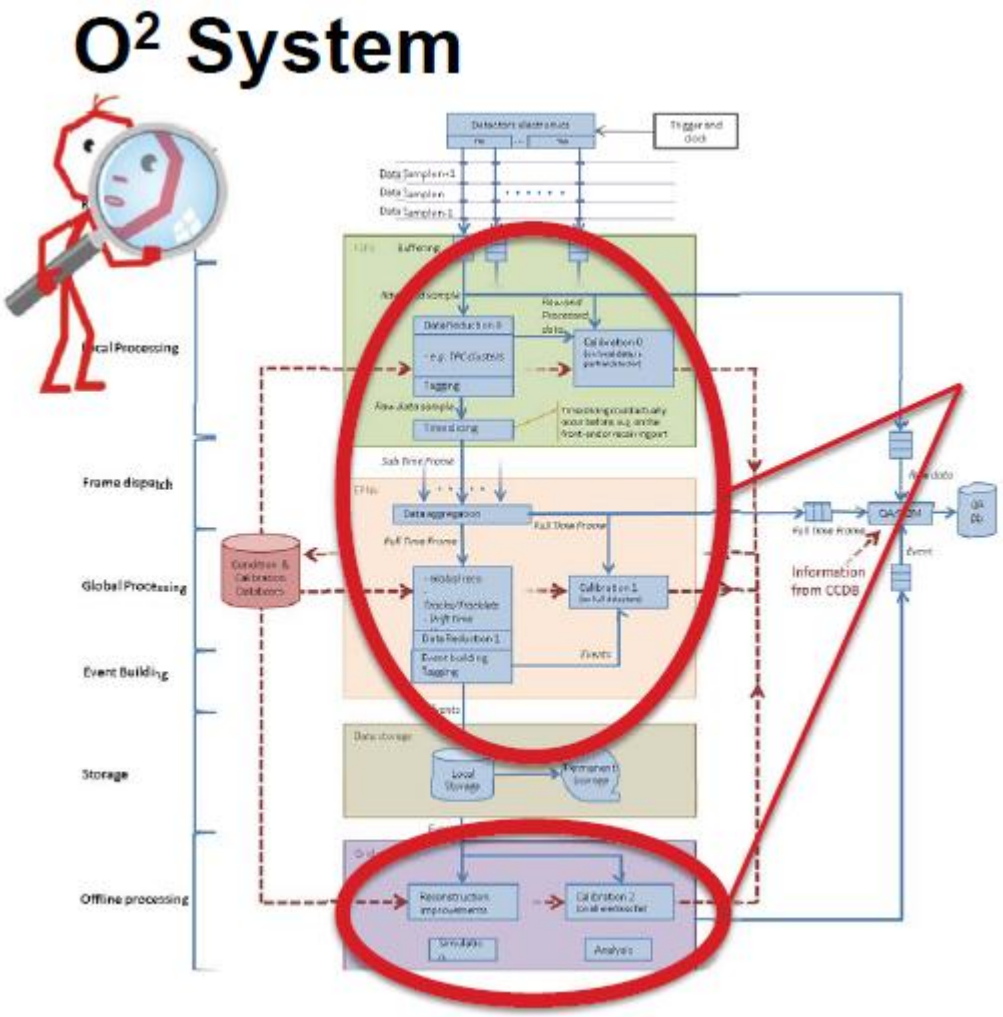


Different technologies/techniques used in DAQ/HLT
e.g. Ethernet <-> Infiniband

Overview of Online-Offline (O^2)



Overview of Online-Offline (O^2)



Networking and Data Transport

- Connect the different computing layers (FLP/EPN)
- Transport of AODs for physics analysis from the O2 farm to the Grid
- Data transfer between grid sites

Requirements of Online-Offline (O^2)

Network Requirements :
Total number of nodes: **~1500**
FLP Node Output: up to **12 Gbit/s**
EPN Node Input: up to **7.2 Gbit/s**
EPN Output: up to **0.5 Gbit/s**

Two technologies available :
- **10/100Gbit** Ethernet (currently used in DAQ)
- **QDR/FDR** Infiniband (40/52Gbit, used in HLT)

Both would allow to construct a network satisfying the requirements even today

Processing Power :
Estimate for online systems based on current HLT processing power
- **~2500** cores distributed over **200** nodes
- **108 FPGAs** on H-RORCs for cluster finding **1 FPGA equivalent to ~80 CPU cores**
- **64 GPGPUs** for tracking (NVIDIA GTX480 + GTX580)

Scaling to 50 kHz rate to estimate requirements :
- **~ 250,000 cores**
- additional processing power by FPGAs + GPGPUs

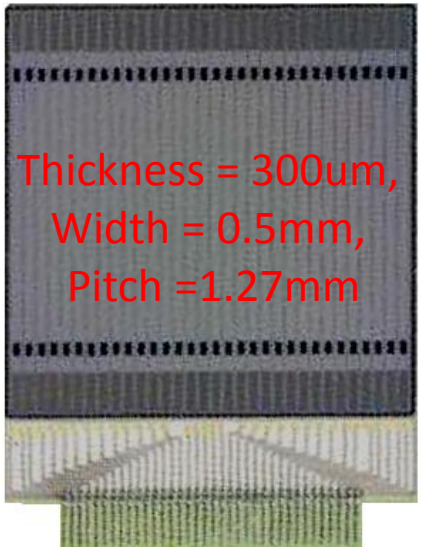
=> **1250-1500 nodes in 2018 with multicores**

Our Participation :: O^2

1. CWG 5: Computing Platform
2. CWG 6: Calibration
3. CWG7 : Reconstruction
4. CWG8 : Simulation
5. CWG9 : QA, DQM, Visualization
6. CWG 12: Computer hardware

FCAL : Development of Detector from Strip to pad detector

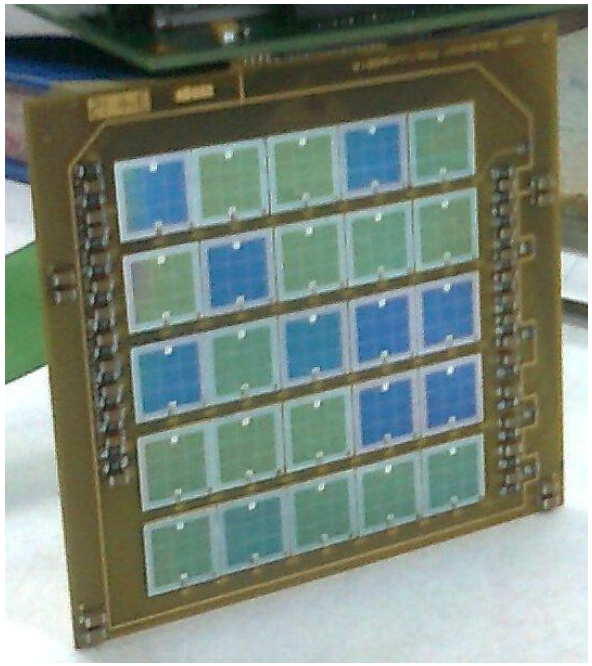
32 channel strips with connector



1.27 mm Pitch connector

Array of 1mm*1mm pixel (Si) detector

(5*5)Array of 1cm*1cm pad(Si) detector



Silicon PAD detector array of dimension (6cm*6cm) each pixel of area1cm^2

New :: to be tested very soon

Participation from ALICE-INDIA Collaboration

Institution / Timeline	PMD Operation	MS Operation& Upgrade	CRU	TPC	MFT	O2	FoCal (Silicon detector develop. testing)	Physics Data Analysis
TIME-LINE	**2013 – 2018**	**2013 – 2018**	**2013– 2018 Install. in LS2**	**2013 - 2018 Install. in LS2**	**2013 – 2018 Install. in LS2**	**2013 – 2018 Install. in LS2**	**2013 – Install. after LS2 subject to approval**	**2013 -**
VECC	**Y**		**Y**	**Y**			**Y**	**Y**
BARC			**Y**				**Y**	
SINP		**Y**	**Y**		**Y**	**Y**		**Y**
IOP	**Y**			**Y**				**Y**
NISER				**Y**				**Y**
Aligarh		**Y**			**Y**			**Y**
Panjab U.	**Y**							**Y**
Gauhati U.								**Y**
IIT-Indore				**Y**			**Y**	**Y**
Jammu U.	**Y**					**Y**	**Y**	**Y**
Rajasthan U.	**Y**							**Y**
Bose Inst.			**Y**	**Y**				**Y**
IIT-B	**Y**			**Y**		**Y**	**Y**	**Y**

Conclusions

ALICE TPC Upgrade

- Successful hands on experience /training .
- GEM detectors will be built in India and tested.
- Our participation to ALICE TPC upgrade will continue
- Our participation will include TPC GEM simulations also.

CRU

- Design exploration for the prototype is underway
- Received one AMC40 card from LHCb for further analysis and examination
- Design for 10 Gigabit Ethernet communication to be tested
- GBT receiver to be implemented
- A firmware design framework for detector specific firmware development has to specified

- CWG 5: Computing Platform
- CWG 6: Calibration
- CWG7 : Reconstruction
- CWG8 : Simulation
- CWG9 : QA, DQM, Visualization
- CWG 12: Computer hardware